

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,970,418	11/13/90	Masterson	—	—	
MA	5,210,715	05/11/93	Houston	—	—	
MA	4,928,265	05/22/90	Higuchi et al.	—	—	
MA	4,953,130	08/28/90	Houston	—	—	
MA	5,251,309	10/05/93	Kinoshita et al.	—	—	
MA	4,099,231	07/01/78	Kotok et al.	—	—	

FOREIGN PATENT DOCUMENTS

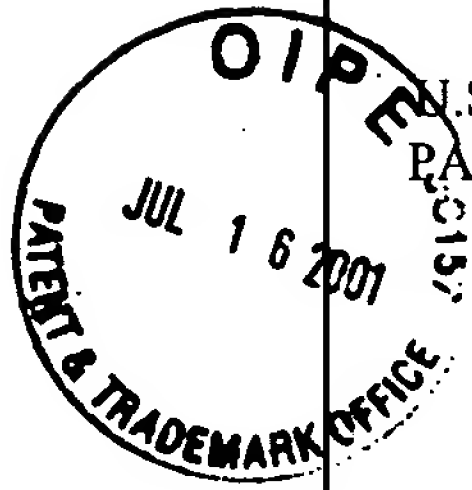
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Hans-Jurgen Mattausch et al., "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length," IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988)
MA	Lineback, J. Robert, "System Snags Shouldn't Slow the Boom in Fast Static RAMs," Electronics, pp. 60-62 (July 23, 1997)
MA	Kanopoulos, Nick and Jill H. Hallenbeck, "A First-In, First-Out Memory for Signal Processing Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)

EXAMINER Glenn June	DATE CONSIDERED 8/8/2003
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



Technology Center 2100

RECEIVED
JUL 18 2001

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	3,691,534	09/12/72	Veradi, et. al	—	—	
MA	3,771,145	11/06/73	Wiener	—	—	
MA	4,536,795	08/20/85	Hirota, et. al	—	—	
MA	4,629,909	12/16/86	Cameron	—	—	
MA	4,631,659	12/23/86	Hayne, et. al	—	—	
MA	4,858,113	08/15/89	Saccardi	—	—	
MA	4,499,536	02/12/85	Gemma et al.	—	—	
MA	4,648,102	03/03/87	Riso, et. al	—	—	

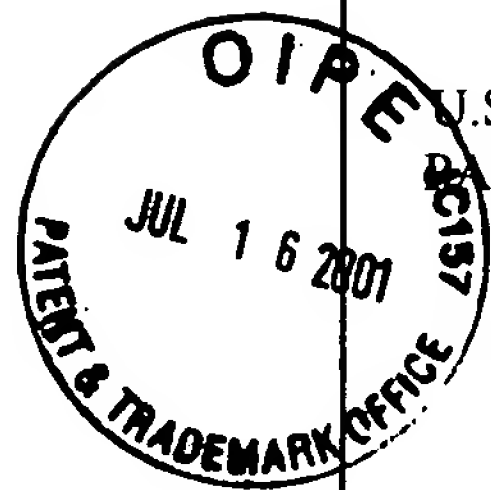
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
MA	EP 0424774	05/02/91	EPO	—	—		
MA	EP 0449052	03/29/90	EPO	—	—		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Takasugi, A. et al., "A Data-Transfer Architecture for Fast Multi-Bit Serial Access Mode DRAM," 11 th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985)
MA	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
MA	Fagan, J.L., "A 16-kbit Nonvolatile Charge Addressed Memory," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5, pp. 631-636 (Oct. 1976)
MA	Schmitt-Landsiedel, Doris, "Pipeline Architecture for Fast CMOS Buffer RAMs," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)

EXAMINER <i>Gilman Arner</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

Technology Center 2100

 RECEIVED
 JUL 18 2001

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,825,287	04/25/89	Baji, et. al	—	—	
MA	4,845,677	07/04/89	Chappell, et. al	—	—	
MA	4,873,671	10/10/89	Kowshik, et. al	—	—	
MA	4,876,670	10/24/89	Nakabayashi, et. al	—	—	
MA	5,179,667	01/12/1993	Iyer	—	—	
MA	4,901,036	02/13/90	Herold, et. al	—	—	

FOREIGN PATENT DOCUMENTS

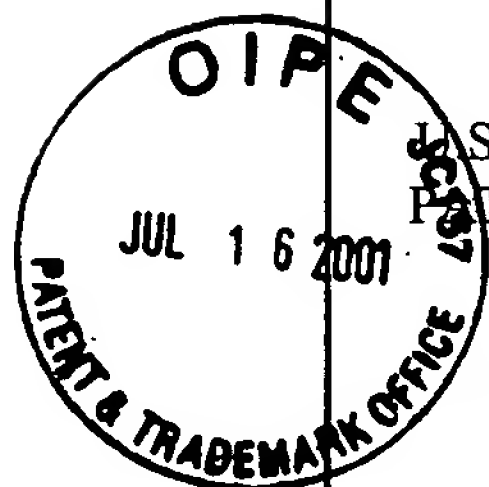
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
MA	EP 0218523	05/30/89	EPO	—	—		
MA	JP-A-1-236494	09/21/89	JP	—	—	YES	
MA	Sho 62-71428	03/27/87	JP	—	—	YES	
MA	EP 0282735	09/21/88	EPO	—	—		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)
M	1989 GaAs IC Data Book & Designers Guide, Gigabit Logic Inc. (Aug 1989)
M	"IC's for Entertainment Electronics, Picture in Picture System Edition 8.89", Siemens AG, 2/89

EXAMINER <i>Chun Han</i>	DATE CONSIDERED 8/8/2007
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



Technology Center 2100

RECEIVED
JUL 18 2001

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
GA	5,099,481	04/24/92	Miller	—	—	
GA	5,016,226	05/14/91	Hiwada, et. al	—	—	
GA	5,023,835	06/11/91	Akimoto, et. al	—	—	
GA	5,036,495	07/30/91	Busch, et. al	—	—	
GA	5,111,486	05/05/92	Oliboni, et. al	—	—	
GA	5,123,100	06/16/92	Hisada, et. al	—	—	

FOREIGN PATENT DOCUMENTS

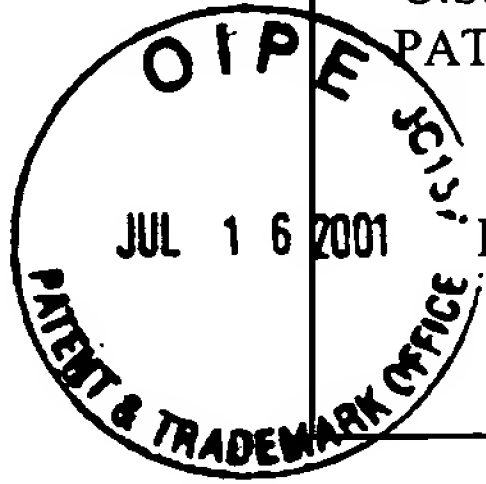
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
GA	WO 89/12936	12/28/89	PCT	—	—	
GA	JP 62-51509	03/06/87	Japan	—	—	YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

GA	Svensson, Christer, "High Speed CMOS Chip to Chip Communications Circuit," IEEE International Symposium on Circuits and Systems, pp. 2228-2231 (Jun. 1991)
GA	Wakayama, Myles, "A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, pp. 1074-1081 (Dec. 1987)
GA	Iqbal, Mohammad Shakaib, "Internally Timed RAMs Build Fast Writable Control Stores," Electronic Design, pp. 93-96 (August 25, 1988)
GA	Schnaitter, William M. et al., "A 0.5-GHz CMOS Digital RF Memory Chip," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
GA	Whiteside, Frank, "A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output," IEEE International Solid-State Circuits Conference Digest (Feb. 1986)
GA	Wu, Jich-Tsornng, "A 100-MHz Pipelined CMOS Comparator," IEEE Journal of Solid-State Circuits, Vol. 23, No. 6, pp. 1379-1385 (Dec. 1988)
GA	Motorola MC88200 Cache/Memory Management Unit User's Manual, Motorola Inc. 1989
GA	B. Ramakrishna et al., "The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs" Computer IEEE, Jan 1989 pp. 12-35

EXAMINER <i>G. L. H. A. H. M.</i>	DATE CONSIDERED <i>8/2/003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	4,755,937	July 5, 1989	Glier	—	—	
BA	4,875,192	Oct 17, 1989	Matsumoto	—	—	

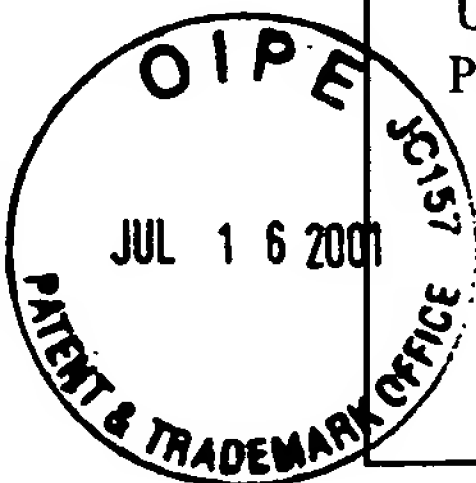
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

BA	Pelgrom et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, vol. sc-22, no. 3, June 1987, pp 415-422
BA	Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pp 1544-1548
BA	Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988
BA	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-10Nov88-doc23, Norsk Data, Oslo, Norway, pp. 1-12, Nov. 10, 1988
M	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-6Jan89-doc31, Norsk Data, Oslo, Norway, pp. 1-24, Jan 6, 1989
BA	Bakka et al., "SCI: Logical Level Proposals", SCI-6Jan89-doc32, Norsk Data, Oslo, Norway, pp. 1-20, Jan 6, 1989
M	Knut Alnes, "Scalable Coherent Interface", SCI-Feb 89-doc52, (To appear in the Eurobus Conference Proceedings May 1989), pp. 1-8
M	Boysel et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pp. 141-146,
BA	Boysel et al., "Random Access MOS Memory Packs More Bits To The Chip", Electronics, Feb. 16, 1970, pp. 109-146,

EXAMINER <i>Glenn Ann</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	5,034,964	Jul. 23, 1991	Khan et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

BA	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
MA	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
MA	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
MA	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20
MA	"High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-14
BA	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83
MA	Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

Technology Center 2100

RECEIVED
JUL 18 2001

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	4,330,852	May 18, 1982	Redwine et al.	—	—	
<i>MA</i>	4,703,418	Oct. 27, 1987	James	—	—	
<i>MA</i>	4,785,394	Nov. 15, 1988	Fischer	—	—	
<i>MA</i>	4,726,021	Feb. 16, 1988	Horiguchi et al.	—	—	
<i>MA</i>	4,870,562	Sept. 26, 1989	Kimoto et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
<i>MA</i>	S56-82961	July 7, 1981	Japan	—	—	YES	
<i>MA</i>	S57-14922	Jan. 26, 1982	Japan	—	—	YES	
<i>MA</i>	Sho 60-80193	May 8, 1983	Japan	—	—	YES	
<i>MA</i>	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES	
<i>MA</i>	S61-72350	April 14, 1986	Japan	—	—	YES	
<i>MA</i>	S63-142445	June 14, 1988	Japan	—	—	YES	
<i>MA</i>	B63-46864	Sept. 19, 1988	Japan	—	—	YES	
<i>MA</i>	S64-29951	Jan. 31, 1989	Japan	—	—	YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
<i>MA</i>	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
<i>MA</i>	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
<i>MA</i>	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
<i>MA</i>	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER <i>Glenn Anre</i>	DATE CONSIDERED <i>8/8/2013</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
JA	4,205,373	May 27, 1980	Shah et al.	—	—	
JA	4,845,670	Jul. 4, 1989	Nishimoto et al.	—	—	
JA	4,509,142	Apr. 2, 1985	Childers	—	—	
JA	4,183,095	Jan. 8, 1980	Ward	—	—	
JA	4,685,088	Aug. 4, 1987	Ianucci	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
JA	0 246 767	April 28, 1987	EPO	—	—	
JA	0 334 552	Mar. 16, 1989	EPO	—	—	
JA	0 276 871	Jan. 29, 1988	EPO	—	—	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JA	European Search Report for EPO Patent Application No. 00 101 1832
JA	European Search Report for EPO Patent Application No. 89 30 2613
JA	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
JA	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
JA	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
JA	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
JA	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
JA	JEDEC Standard No. 21C

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>DA</i>	4,630,193	Dec. 16, 1986	Kris	—	—	
<i>HA</i>	4,710,904	Dec. 1, 1987	Suzuki	—	—	
<i>MA</i>	4,739,502	Apr. 19, 1988	Nozaki	—	—	
<i>MA</i>	4,905,201	Feb. 27, 1990	Ohira et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>DA</i>	European Search Report for EPO Patent Application No. 00 10 0018
<i>MA</i>	European Search Report for EPO Patent Application No. 00 10 822

EXAMINER <i>Glenn Anre</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

RECEIVED

JUL 18 2001

Technology Center 2100

OIP
JUL 1
PATENT & TRADEMARK OFFICEOIP
JUL 16 2001
PATENT & TRADEMARK OFFICE



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

Technology Center 2100
JUL 18 2001

RECEIVED

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,445,204	04/24/84	Nishiguchi	—	—	
MA	4,821,226	04/11/89	Christopher et al.	—	—	
MA	4,882,712	11/21/89	Ohno et. al.	—	—	
MA	4,951,251	08/21/90	Yamaguchi et al.	—	—	
MA	4,928,265	12/29/92	Higuchi Beighe et al.	—	—	
MA	5,107,465	04/21/92	Fung et al.	—	—	

Per E
Per MA

FOREIGN PATENT DOCUMENTS

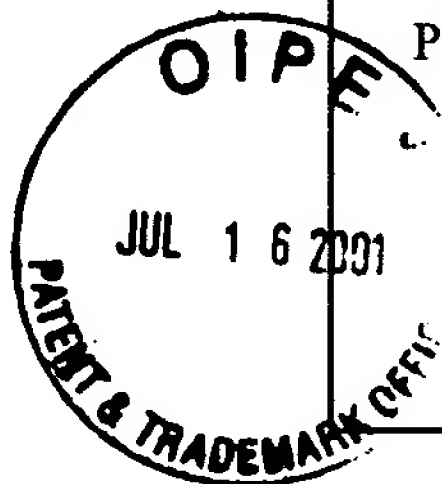
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO N YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
MA	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
MA	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)

EXAMINER <i>Gylean Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



Technology Center 2100
JUL 18 2001

RECEIVED

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>Per Ke</i> <i>Per M</i> <i>JA</i>	5 4,206,833	04/27/93	Lee	—	—	
<i>JA</i>	4,953,128	08/28/90	Kawai et al.	—	—	
<i>JA</i>	5,140,688	08/18/92	White et al.	—	—	
<i>JA</i>	5,018,111	05/21/91	Madland	—	—	
<i>JA</i>	4,845,664	07/04/89	Aichelmann, Jr. et al.	—	—	
<i>JA</i>	4,734,880	03/29/88	Collins	—	—	

FOREIGN PATENT DOCUMENTS

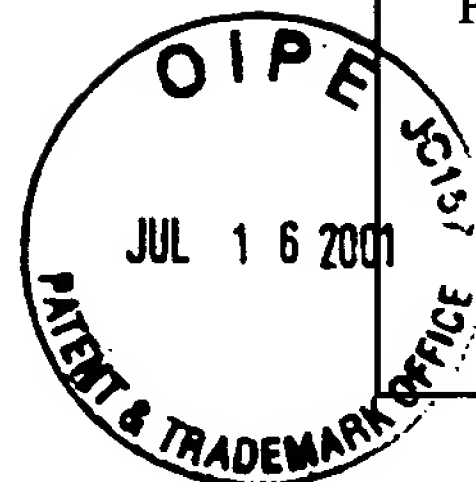
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO N YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>JA</i>	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5- μ m Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
<i>JA</i>	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
<i>JA</i>	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
<i>JA</i>	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
<i>JA</i>	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
<i>JA</i>	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
<i>JA</i>	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
<i>JA</i>	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
<i>JA</i>	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)

EXAMINER <i>Glenn Auve</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,183,095	01/08/80	Ward	—	—	
MA	4,975,872	12/04/90	Zaiki	—	—	
MA	5,016,226	05/14/91	Hiwada et al.	—	—	
MA	4,853,896	08/01/89	Yamaguchi	—	—	
MA	4,747,079	05/24/88	Yamaguchi	—	—	
MA	4,945,516	07/31/90	Kashiyama	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO N YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)
MA	K. Numata et. al. "New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)
MA	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
MA	J. Sonntag et al. "A Monolithic CMOS 10MHz DPLL for Burst-Mode Data Retiming", IEEE International Solid State Circuits Conference (ISSCC) February 16, 1990

EXAMINER Glenna Anne	DATE CONSIDERED 8/8/2003
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

Technology Center 2100
JUL 18 2001

RECEIVED

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,649,511	03/10/97	Gdula	—	—	
DA	4,860,198	08/22/89	Takenaka	—	—	
DA	3,969,706	07/13/76	Proebsting et al.	—	—	
DA	4,766,536	08/23/88	Wilson, Jr. et al.	—	—	
DA	4,998,262	03/05/91	Wiggers	—	—	
DA	4,757,473	07/12/88	Kurihara et al.	—	—	
DA	4,792,926	12/20/88	Roberts	—	—	
DA	4,811,202	03/07/89	Schabowski	—	—	
DA	5,034,917	07/23/91	Bland et al.	—	—	
DA	5,301,278	04/05/94	Bowater et al.	—	—	
DA	5,153,856	10/06/92	Takahashi	—	—	
DA	4,845,670	07/04/89	Nishimoto et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO N YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DA	M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)
DA	R. L. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Coding Applications", IEEE Transactions on Circuits And Systems, vol. 36 No. 10, pp. 1275-1280 (Oct 1989)
DA	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. SC-18 No. 5, pp. 561-567 (Oct. 1983)
DA	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989)

EXAMINER Glenn Anne	DATE CONSIDERED 8/8/2003
------------------------	-----------------------------

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	4,685,088	08/04/87	Iannucci	—	—	
BA	4,509,142	04/02/85	Childers	—	—	
BA	5,051,889	09/24/91	Fung et al.	—	—	
BA	5,361,277	11/01/94	Grover	—	—	
BA	4,954,987	09/04/90	Auvinen et al.	—	—	
BA	4,570,220	02/11/86	Tetrick et al.	—	—	
BA	4,247,817	01/27/81	Heller	—	—	
BA	4,519,034	05/21/85	Smith et al.	—	—	
BA	3,691,534	09/12/72	Varadi et al.	—	—	
BA	4,920,486	04/24/90	Nielsen	—	—	
BA	4,263,650	04/21/81	Bennett et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO N YES/NO
BA	0 276 871	03/08/88	DE FR GB IT EPX	—	—	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

BA	S.K. Kwon et al., "Memory Chip Organizations For Improved Reliability In Virtual Memories", IBM Technical Bulletin vol. 25 No. 6, pp. 2952-2957 (Nov 1982)
BA	J. Peterson, "System-Level Concerns Set Performance Gains", High Performance Systems, pp. 71-77 (Sept. 89)
BA	N. Margulis, "Single Chip CPU Eases Single Chip System Design", High Performance Systems, pp. 34-44 (Sept. 89)
BA	F.Nart, "Multiple Chips Speed CPU Subsystems", High Performance Systems, pp. 46-55 (Sept. 89)
BA	D.T. Wong, "An 11-ns 8Kx18 CMOS Static RAM with 0.5-um Devices", IEEE Journal of Solid State Circuits, vol. 23, No. 5, pp. 1095-1103 (Oct. 1988)
BA	A. Agarwal et al., "An Evaluation of Directory Schemes for Cache Coherence", IEEE, pp. 280-289, 1988

EXAMINER

Glenn Anne

DATE CONSIDERED

8/8/2003

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	4,719,602	01/12/88	Hag et al.	—	—	
<i>MA</i>	5,023,488	06/11/91	Gunning	—	—	
<i>MA</i>	4,754,433	06/28/88	Chin et al.	—	—	
<i>MA</i>	3,771,145	11/06/73	Wiener	—	—	
<i>MA</i>	5,021,985	06/04/91	Hu et al.	—	—	

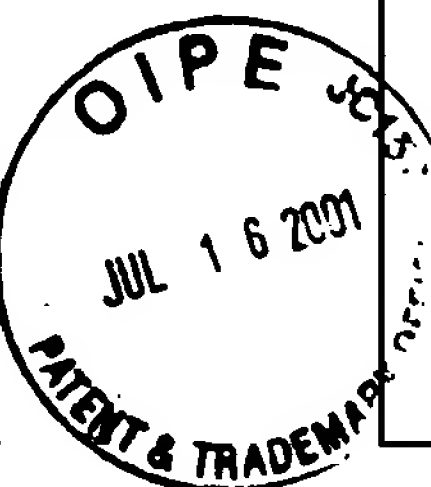
FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO N YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	T. L. Jeremiah, "SYNCHRONOUS LSSD PACKET SWITCHING MEMORY AND I/O CHANNEL", IBM Technical Bulletin vol. 24 No. 10, pp. 4986-4987 (March 1982)
<i>MA</i>	D. Hawley, "Superfast Bus Supports Sophisticated Transactions", High Performance Systems, pp. 90-94 (Sept. 89)
<i>MA</i>	M. Bazes, A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. SC-18, No. 2, pp. 164-172 (April 1983)
<i>MA</i>	D. Wendell et al., "A 3.5ns Self Timed SRAM", IEEE 1990 Symposium on VLSI Circuits pp. 49-50
<i>MA</i>	J. Chun et al., "A pipelined 650 MHz GaAs 8K ROM with Translation Logic" IEEE 1990 GaAs IC Symposium, pp 139-142
<i>MA</i>	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989)

EXAMINER <i>Glen Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	4,633,735	05/05/87	Novak, et. al	—	—	
<i>MA</i>	5,684,753	11/04/97	Hashimoto, et al	—	—	
<i>MA</i>	4,322,635	03/30/81	Redwine	—	—	
<i>MA</i>	4,916,670	04/10/90	Suzuki et al.	—	—	
<i>MA</i>	5,006,982	04/09/91	Ebersole et al.	—	—	
<i>MA</i>	4,636,986	01/13/87	Pinkham	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4MB Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
<i>MA</i>	Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985)
<i>MA</i>	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
<i>MA</i>	Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984)
<i>MA</i>	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976)
<i>MA</i>	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
<i>MA</i>	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)

EXAMINER <i>Glen Ave</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED

JUL 18 2001

Technology Center 2100



U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,979,145	12/18/90	Remington et al.	—	—	
MA	5,276,846	01/04/94	Aichelmann Jr., et. al	—	—	

FOREIGN PATENT DOCUMENTS

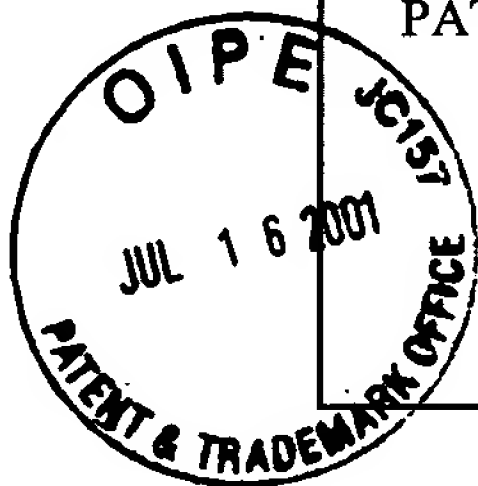
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
MA	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
MA	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
MA	Dave Bursky, "ADVANCED SELF-TIMED SRAM PARES ACCESS TIME TO 5 NS", Electronic Design, pp. 145-147 (Feb. 22, 1990)

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>8/8/2002</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>MA</i>	SHO 58-192154	Nov. 9, 1983	Japan	<i>—</i>	<i>—</i>	NO
<i>MA</i>	SHO 63-34795	Feb. 15, 1988	Japan	<i>—</i>	<i>—</i>	NO
<i>MA</i>	SHO 61-107453	May 26, 1986	Japan	<i>—</i>	<i>—</i>	NO
<i>MA</i>	SHO 63-91766	April 22, 1988	Japan	<i>—</i>	<i>—</i>	YES
<i>MA</i>	SHO 62-16289	Jan. 24, 1987	Japan	<i>—</i>	<i>—</i>	NO
<i>MA</i>	SHO 61-160556	Oct. 4, 1986	Japan	<i>—</i>	<i>—</i>	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER <i>Glen Ann</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
JA	4,482,999	11/13/84	Janson et al.	—	—	
MA	5,029,124	07/02/91	Leahy et al.	—	—	
JA	5,193,193	03/09/93	Iyer	—	—	
JA	4,926,385	05/15/90	Fujishima et al.	—	—	
JA	4,566,099	01/21/86	Magerl	—	—	
MA	4,803,621	02/07/89	Kelly	—	—	
JA	4,589,108	05/13/86	Billy	—	—	
JA	4,870,622	09/26/89	Aria et al.	—	—	
JA	4,878,166	10/31/89	Johnson et al.	—	—	
JA	4,849,965	07/18/89	Chomel et al.	—	—	
JA	4,851,990	07/25/89	Johnson et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER <i>Graham Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



RECEIVED
JUL 18 2001
Technology Center 2100

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181



RECEIVED
JUL 18 2001
Technology Center 2100

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	4,528,661	07/09/85	Bahr et al.	—	—	
BA	4,048,673	09/13/77	Hendrie et al.	—	—	
BA	4,748,617	05/31/88	Drewlo	—	—	
BA	4,839,801	06/13/89	Nicely et al.	—	—	
BA	4,949,301	08/14/90	Joshi et al.	—	—	
BA	3,950,735	04/13/76	Patel	—	—	
BA	4,047,246	09/06/77	Kerllenevich et al.	—	—	
BA	4,763,249	08/09/88	Bomba et al.	—	—	
BA	4,625,307	11/25/86	Tulpule et al.	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

#6

1 of 1



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

Technology Center 2100

DEC 20 2001

RECEIVED

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,933,953	Jun. 12, 1990	Yagi	-	-	
MA	5,133,064	Jul. 21, 1992	Hotta et al	-	-	
MA	5,184,027	Feb. 2, 1993	Masuda et al.	-	-	

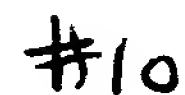
FOREIGN PATENT DOCUMENTS


EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
MA	JP 1284132	Nov 15, 1989	Japan	-	-	yes
MA	EP 0 329 418 A2	Aug 23, 1989	EPO	-	-	
MA	JP 1043894	Feb. 16, 1989	Japan	-	-	yes

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	"Intel MCS-4 Micro Computer Set", Intel Corporation, Santa Clara, CA, 1972, (pp.1-12)
MA	"MIPS R3010 coprocessor", IEEE Micro June 1988, (pp.54-62)
MA	"Intel MCS-4 Micro Computer Set Users Manual", Intel Corporation, Santa Clara, CA, March 1972, (pp.1-26, and 60-68)
MA	"Bipolar/MOS Memories Data Book", Advanced Micro Devices, Sunnyvale, CA, 1986 (pp. 4-143 to 4-163)
MA	"Memories 1986-87 Databook", Fujitsu Inc., 1986 (pp. 1-102 to 1-128)
MA	H. J. Mattausch, et al., "A Memory-Based High-Speed Digital Delay Line With a Large Adjustable Length", IEEE Journal of Solid State Circuits, vol. 23, no. 1, Feb. 1988 (pp. 105-110)

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



 <p>U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p>	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

<u>EXAMINER INITIALS</u>	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,761,567	Aug. 2, 1988	Walters, Jr. et al.	307	269	
MA	5,101,117	Mar. 31, 1992	Johnson et al.	307	269	

FOREIGN PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
MA	sho 58-31637A	Feb 24 , 1983	Japan	/	/	
MA	sho 59-165285A	Mar. 11, 1983	Japan	/	/	
MA	sho 60-261095A	June 6, 1984	Japan	/	/	
MA	sho 63-300310	Dec. 7, 1988	Japan	/	/	
MA	hei 2-8950	Jan 12, 1990	Japan	/	/	
MA	sho 58-184626A	Oct 28, 1983	Japan	/	/	

RECEIVED

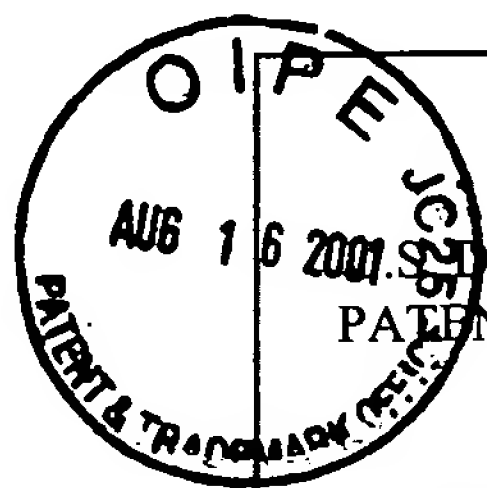
JAN 22 2002

Technology Center

OTHER DOCUMENTS (Inventory Number, Title, Date, Portion Types, etc.)	

EXAMINER <i>Glenn Anre</i>	DATE CONSIDERED <i>8/8/2003</i>
----------------------------	---------------------------------

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C15	SERIAL NUMBER 09/835,263
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 13, 2001	GROUP ART UNIT 2181

RECEIVED

AUG 20 2001

Technology Center 2100

DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	"MIPS Chip Set Implements Full ECL CPU" Microprocessor Report, MicroDesign Resources Inc., Vol. 3: No. 12; Dec. 1989
MA	"R6000 System Bus & R6020 SBC Specification" MIPS Computer Systems Inc., Sunnyvale, CA, Aug 22, 1989
MA	R.A. Volz et al., "POSITION PAPER ON GLOBAL CLOCK FOR THE FUTUREBUS +", SCI - 1989 - doc-59, pp. 1-9
MA	"ECL bus controller hits 266 Mbytes/s" Microprocessor Report, MicroDesign Resources Inc., Vol. 4: No. 1; Pg. 12, Jan. 24, 1990

EXAMINER <i>Gilma Anne</i>	DATE CONSIDERED <i>8/8/2003</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	